Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-19. (Cancelled)

20. (Currently Amended) A portion of a wrap-around-gated field-effect transistor formed on a handle wafer, the portion comprising:

an silicon-on-insulator (SOI) island comprising ~~side surfaces forming~~ a surface periphery with a surface facing toward the handle wafer, the SOI island [[and]] extending, for a length, along a major axis in [[the]] a horizontal direction; and

a gate electrode surrounding and supporting the SOI island, the gate electrode extending in a vertical direction from [[a]] the handle wafer, [[and]] the gate electrode having a thickness, in the horizontal direction, less than the length of the SOI island such that a first portion of the SOI island extends on one side of the gate electrode and ~~another~~ a second portion of the SOI island extends on another side of the gate electrode, and the gate electrode extending entirely around the surface periphery of the SOI island such that a portion of the gate electrode is between the surface of the SOI island and the handle wafer.

21. (Original) The portion according to claim 20, wherein a first edge face of the SOI island extends outward on one side of the gate electrode and a second edge face of the SOI island extends oppositely outward on another side of the gate electrode.

22. (Original) The portion according to claim 20, wherein the gate electrode has a cross-sectional profile that is C-shaped.

23. (Original) The portion according to claim 20, wherein a portion of a top surface of the SOI island is exposed.

24. (Original) The portion according to claim 20, wherein at least a portion of SOI island is supported underneath by an oxide layer on the handle wafer.

25. (Currently Amended) A field-effect-transistor formed on a handle wafer, the field-effect-transistor comprising:

[[a]] an silicon-on-insulator (SOI) island comprising a surface periphery with a surface facing toward the handle wafer and two edge faces, the SOI island oriented substantially in a horizontal direction;

a wrap-around gate electrode oriented in substantially a vertical direction intersecting with the SOI island ~~in-between~~ between the two edge faces such that a first portion of the SOI island extends on one side of the gate electrode and a second portion of the SOI island extends on another side of the gate electrode, and the wrap-around gate electrode ~~extends~~ extending entirely around the surface periphery of the SOI island such that a portion of the gate electrode is between the surface of the SOI island and the handle wafer;

a source region formed ~~on a first part~~ in the first portion of the SOI island~~, on one side of the gate electrode~~; and

a drain region formed ~~on a second part~~ in the second portion of the SOI island~~, on another side of the gate electrode~~.

26. (Currently Amended) The field-effect transistor of claim 25, wherein a portion of a bottom surface of at least one of the first portion of the SOI island or the second portion of the SOI island ~~on both sides of the gate electrode~~ is exposed.

27. (Currently Amended) The field-effect transistor of claim 25, wherein at least [[a]] one of the first portion of the SOI island or the second portion of the SOI island is supported underneath by an oxide layer.

28. (Cancelled)